Listing of Claims

Claim 1 (currently amended): A clock system for distributing and generating a digital clock signal for a plurality of electronic assemblies, the clock system ~~including~~ comprising:

a ~~remote fixed frequency~~ reference clock for generating a first clock signal of a first frequency;

control circuitry for generating a sync signal, the sync signal being associated with a reference edge of the first clock signal;

~~a plurality of local~~ clock modules respectively disposed on the plurality of electronic assemblies, the ~~local~~ clock modules including synthesizer circuitry for ~~creating a~~ generating at least one second ~~variable~~ clock signal having ~~of a~~ one or more second frequencies, wherein at least one of the second frequencies is different ~~frequency than~~ from the first frequency; and

fanout circuitry coupled ~~between~~ to the ~~remote fixed frequency~~ reference clock and the ~~plurality of local~~ clock modules to distribute the first clock signal and the sync signal.

Claim 2 (currently amended): [[A]] The clock system according to claim 1, wherein[[:]] the clock modules further comprise phase-locked-loop circuitry and wherein the synthesizer circuitry comprises a direct-digital-synthesizer having an input for receiving the first clock signal ~~of a first frequency,~~ and an output coupled to the [[a]] phase-locked-loop circuitry ~~disposed at the output of the synthesizer~~.

Claim 3 (currently amended): A clock system ~~according to claim 1~~ for distributing and generating a digital clock signal for a plurality of electronic assemblies, the clock system comprising:

a reference clock for generating a first clock signal of a first frequency;

clock modules respectively disposed on the plurality of electronic assemblies, the clock modules including synthesizer circuitry for generating at least one second clock signal having one or more second frequencies, wherein at least one of the second frequencies is different from the first frequency;

fanout circuitry coupled between the reference clock and the clock modules to distribute the first clock signal; and ~~further including:~~

control circuitry for generating a sync signal, the sync signal being associated with a ~~predetermined~~ reference edge from the first clock signal, the fanout circuitry including parallel connections for distributing the sync signal with the first clock signal, [[;]] and the ~~local~~ clock modules including synchronization circuitry for aligning and starting the ~~local~~ clock modules synchronously[[,]] based on ~~the clock edge associated with~~ the sync signal.

Claim 4 (currently amended): [[A]] The clock system according to claim 2, wherein[[:]] the synthesizer and the phase-locked-loop circuitry cooperate to generate [[a]] the at least one second clock signal and at least one of the ~~of a~~ second ~~frequency~~ frequencies is greater than the first frequency.

Claim 5 (currently amended): [[A]] The clock system according to claim 1, wherein[[:]] the plurality of electronic assemblies include respective pattern generators having clock inputs ~~tied~~ coupled to the outputs of the respective clock modules.

Claim 6 (currently amended): [[A]] The clock system according to claim [[5]] 1, wherein[[:]] at least two of the ~~clock modules generate local clocks of different~~ second frequencies ~~for the respective pattern generators~~ are different from one another.

Claim 7 (currently amended): A clock system ~~according to claim 6~~ for distributing and generating a digital clock signal for a plurality of electronic assemblies, the clock system comprising:

a reference clock for generating a first clock signal of a first frequency;

clock modules respectively disposed on the plurality of electronic assemblies, the clock modules including synthesizer circuitry for generating second clock signal having second frequencies, wherein at least one of the second frequencies is different from the first frequency and at least two of the second frequencies are different from one another;

pattern generators respectively disposed on the plurality of electronic assemblies, the pattern generators having clock inputs coupled to the outputs of the respective clock modules;

fanout circuitry coupled between the reference clock and the clock modules to distribute the first clock signal; and ~~further including:~~

coincidence point detection circuitry for determining synchronous operation between the respective pattern generators.

Claim 8 (currently amended): A frequency-based semiconductor tester ~~including~~ comprising:

~~a computer workstation;~~

a testhead ~~having~~ comprising:

~~remote fixed-frequency clocking~~ reference clock circuitry for ~~creating~~ generating a ~~high-accuracy~~ first clock signal of a first frequency, ~~the testhead coupled to the computer workstation and further including~~

control circuitry for generating a sync signal, the sync signal being associated with a reference edge of the first clock signal,

clock modules ~~a plurality of channel cards, each of the channel cards including~~ having synthesizer circuitry for ~~creating a local frequency based~~ generating at least one second ~~variable~~ clock signal having one or more second frequencies, wherein at least one of the second frequencies is different from ~~of a higher frequency than~~ the first frequency, [[;]] and

fanout circuitry ~~disposed between~~ coupled to the ~~channel card~~ synthesizer circuitry and the ~~fixed-frequency clocking~~ reference clock circuitry for distributing the ~~high-accuracy~~ first clock signal as a reference signal for the synthesizer circuitry and the sync signal.

Claim 9 (currently amended): [[A]] The frequency-based semiconductor tester ~~according~~ according to claim 8, wherein[[:]] the clock modules further comprise phase-locked-loop circuitry and wherein the synthesizer circuitry comprises a direct-digital-synthesizer having an input for receiving the first clock signal ~~of a first frequency,~~ and an output coupled to the [[a]] phase-locked-loop circuitry ~~disposed at the output of the synthesizer~~.

Claim 10 (currently amended): A ~~clock system~~ frequency-based semiconductor tester ~~according to claim 8~~ comprising:

a testhead comprising:

reference clock circuitry for generating a first clock signal of a first frequency,

clock modules having synthesizer circuitry for generating at least one second clock signal having one or more second frequencies, wherein at least one of the second frequencies is different from the first frequency,

fanout circuitry disposed between the synthesizer circuitry and the reference clock circuitry for distributing the first clock signal as a reference signal for the synthesizer circuitry, and ~~further including~~

control circuitry for generating a sync signal, the sync signal being associated with a ~~predetermined~~ reference edge from the first clock signal, the fanout circuitry including parallel connections for distributing the sync signal with the first clock signal, [[;]] and the ~~local~~ clock modules including synchronization circuitry for aligning and starting the ~~local~~ clock modules synchronously[[,]] based on ~~the clock edge associated with~~ the sync signal.

Claim 11 (currently amended): ~~A clock system~~ The frequency-based semiconductor tester according to claim 9, wherein[[:]] the synthesizer and the phase-locked-loop circuitry cooperate to generate [[a]] the at least one second clock signal and at least one of the ~~of a~~ second ~~frequency~~ frequencies is greater than the first frequency.

Claim 12 (currently amended): ~~A clock system~~ The frequency-based semiconductor tester according to claim 8, wherein[[:]] the testhead further comprises a ~~the~~ plurality of ~~electronic assemblies include respective~~ pattern generators having clock inputs ~~tied~~ coupled to the outputs of the respective clock modules.

Claim 13 (currently amended): ~~A clock system~~ The frequency-based semiconductor tester according to claim ~~12~~ 8, wherein[[:]] at least two of the ~~clock modules generate local clocks of different~~ second frequencies ~~for the respective pattern generators~~ are different from one another.

Claim 14 (currently amended): A ~~clock system~~ frequency-based semiconductor tester ~~according to claim 13~~ comprising:

a testhead comprising:

reference clock circuitry for generating a first clock signal of a first frequency,

clock modules having synthesizer circuitry for generating second clock signals having second frequencies, wherein at least one of the second frequencies is different from the first frequency and at least two of the second frequencies are different from one another,

fanout circuitry disposed between the synthesizer circuitry and the reference clock circuitry for distributing the first clock signal as a reference signal for the synthesizer circuitry,

pattern generators having clock inputs coupled to the outputs of the respective clock modules, and ~~further including:~~

coincidence point detection circuitry for determining synchronous operation between the respective pattern generators.

Claim 15 (currently amended): A method of clocking a plurality of electronic assemblies~~, the method including the steps of~~ comprising:

~~remotely establishing~~ generating a ~~fixed~~ first clock signal of a first frequency;

generating a sync signal, the sync signal being associated with a reference edge of the first clock signal,

~~fanning out~~ distributing the ~~fixed~~ first clock signal and the sync signal to a plurality of clock modules disposed on the plurality of electronic assemblies; and

~~synthesizing~~ generating at least one second clock signal with ~~on~~ the plurality of ~~electronic assemblies~~ clock modules, the at least one second clock signal ~~the fixed clock signal to locally create a higher~~ having one or more second frequencies wherein at least one of the second frequencies is different from the first frequency ~~clock signal for each of the electronic assemblies~~.

Claim 16 (currently amended): A method of starting a plurality of ~~ATE~~ automated test equipment pattern generators synchronously, the pattern generators disposed on respective ~~channel cards~~ electronic assemblies, the method ~~including the steps of~~ comprising:

~~creating~~ generating a ~~remote fixed frequency~~ first clock signal of a first frequency;

generating a control sync signal, the sync signal associated with a ~~predetermined~~ reference edge of the ~~fixed frequency~~ first clock signal;

~~fanning out~~ distributing the ~~fixed frequency~~ first clock signal and the sync signal to a plurality of clock modules ~~residing~~ disposed on the respective ~~channel cards~~ electronic assemblies, the clock modules including clock synthesizer circuitry and edge prediction ~~logic~~ circuitry;

~~locally synthesizing a variable frequency~~ generating at least one second clock signal on ~~each of~~ the ~~channel cards~~ clock modules with the respective ~~clock module~~ synthesizer circuitry, the ~~variable frequency~~ at least one second clock signal having one or more second frequencies wherein at least one of the second frequencies is ~~of a~~ different from the first frequency ~~than the fixed frequency clock~~; and

passing the sync signal ~~with~~ through the edge prediction circuitry ~~through the first clock domain to the second variable frequency clock domain~~ to identify ~~an accurate and common~~ start ~~time~~ times for the plurality of pattern generators.

Claim 17 (currently amended): [[A]] The method ~~of starting a plurality of ATE pattern generators~~ according to claim 16, wherein at least two of the pattern generators operate at ~~different~~ frequencies different from one another and receive ~~different variable frequency~~ the second clock signals from the respective clock modules, the method further ~~including the steps of~~ comprising:

detecting coincidence points between the ~~different variable frequency~~ second clock signals; and

utilizing the detected coincidence points to identify starting times for the plurality of pattern generators.

Claim 18 (currently amended): [[A]] The method ~~of starting a plurality of ATE pattern generators synchronously~~ according to claim 16, wherein the ~~clock module~~ synthesizer circuitry includes a plurality of direct-digital-synthesizers, and the step of ~~locally synthesizing~~ generating at least one second clock signal further ~~includes the step of:~~ comprises

aligning the direct-digital-synthesizers.